UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/629,966	07/31/2000	Moshe Gefen	246/68	4504

7590 01/13/2004

Dr. Mark Friedman Ltd
C/O BILL POLKINGHORN - DISCOVER DISPATCH
9003 FLORIN WAY
UPPER MARLBORO, MD 20772

EXAMINER	
ANDERSON, MATTHEW D	

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 01/13/2004

6

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/629,966	GEFEN ET AL.	
	Examiner	Art Unit	
	Matthew D. Anderson	2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136 (a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 December 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claims _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

11)☒ The proposed drawing correction filed on *22 December 2003* is: a)☒ approved b)☐ disapproved.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

15)☐ Notice of References Cited (PTO-892)
16)☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
17)☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
18)☐ Interview Summary (PTO-413) Paper No(s). _____ .
19)☐ Notice of Informal Patent Application (PTO-152)
20)☐ Other: .

DETAILED ACTION

Drawings

1. The drawings were received on 12/22/03. These drawings are approved.

Response to Amendment

2. In response to the amendment filed 12/22/03:

claims 1, 6, 10, 13, and 14 have been amended, and the corresponding objections and rejections have been withdrawn;

claims 2, 7-9, 11-12, and 15 have been canceled;

new claims 17-28 have been added.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

4. Claims 1, 3-4 and 6, 10, 13-14, and 16-28 are rejected under 35 U.S.C. 102(e) as being anticipated by See *et al.* (US Patent # 6,189,070).

5. With respect to claims 1, 3, and 13-14, See *et al.* disclose:

a host for accessing a non-volatile memory device, as shown by processor 100 of figure 1;

a non-volatile flash array for holding code and data, as disclosed in the abstract and column 1, lines 37-39;

non-volatile circuitry for controlling content and activity of the non-volatile array, as shown by the erase, program, and read circuitry (items 190, 194, and 196 of figure 7);

logic circuit hardware, separate from the host, for enabling automatic suspending and/or automatic resuming of operations in response to a read request, as shown by the suspend circuitry (item 192 and 195) which is part of the flash device of figure 7, which is separate from the processor in figure 1, while column 3, lines 55-58, which recites a method and apparatus for suspending a non-read operation in a nonvolatile writeable memory in order to read code from the nonvolatile writeable memory.

6. With respect to claim 4, See *et al.* disclose the logic circuit enabling code execution and data storage/processing facilities within a single chip device with a single silicon die, as disclosed in the abstract and figure 5.

7. With respect to claim 6, See *et al.* disclose the logic circuit being embedded into a memory chip, as shown in figure 5.

8. With respect to claims 10 and 13, See *et al.* disclose the logic circuit monitoring the status of the current operations in the memory chip, as shown by the read status circuitry (item 198 in figure 7).

9. With respect to claim 13, See *et al.* disclose:

adding at least one logic circuit to operate with the non-volatile memory device, as shown by the control circuitry in figures 6 and 7;

monitoring status of current operations in said memory chip by said at least one logic circuit; as shown by the read status circuitry (item 198 in figure 7);

signaling if the device is available for code execution, by said at least one logic circuit, as shown by the suspend and resume latches in figure 7;

commanding the device to suspend and/or resume chip operations, in response to a read request by said at least one logic circuit, by teaching in column 3, lines 55-58, which recites a method and apparatus for suspending a non-read operation in a nonvolatile writeable memory in order to read code from the nonvolatile writeable memory.

10. With respect to claim 14, See *et al.* disclose

adding at least one logic circuit to work with the a non-volatile memory device, as shown by the control circuitry in figures 6 and 7;

sensing read requests while the device is in program/erase mode/operation by the at least one logic circuit, and in response to the sensing, entering of program and/or erase operations into suspend mode, by teaching in column 3, lines 55-58, which recites a method and apparatus for suspending a non-read operation in a nonvolatile writeable memory in order to read code from the nonvolatile writeable memory;

signaling to CPU/BUS to delay executing said read request, by said at least one logic circuit, turning off signal to allow CPU/BUS to execute said read request, by the at least one logic device, exiting of said device from said suspended mode to continue program/erase operation, by said at least one logic circuit, by teaching in figure 4A-B and in column 3, lines 15-

25, enabling and disabling interrupts to allow read and non-read operations, and a check for occurrences of interrupts.

11. With respect to claim 16, See *et al.* disclose suspend/resume logic circuitry for enabling hardware initiated suspending/resuming of data processing operations, as shown by the suspend circuitry (item 192 and 195 in figure 7).

12. With respect to claim 17, See *et al.* disclose a non-volatile memory (150), circuitry for read, programming, and erasing said non-volatile memory (140), and a hardware mechanism for suspending an activity of said circuitry in response to at least one read request (column 3, lines 55-58).

13. With respect to claim 18, See *et al.* disclose the hardware mechanism also is operative to resume said activity of the circuitry after said circuitry has finished processing said at least one read request, as shown by the resume latches in figure 7.

14. With respect to claim 19, See *et al.* disclose the activity being erasing the non-volatile memory, as shown by the erase latches in figure 7.

15. With respect to claim 20, See *et al.* disclose the activity being programming the non-volatile memory, as shown by the program latches in figure 7.

16. With respect to claim 21, See *et al.* disclose the hardware mechanism includes at least one logic circuit, as shown in figure 7.

17. With respect to claim 22, See *et al.* disclose:

indicating to a host that issued said at least one read request that execution of the read request should be delayed, by teaching in column 3, lines 55-58, which recites a method and

apparatus for suspending a non-read operation in a nonvolatile writeable memory in order to read code from the nonvolatile writeable memory;

and subsequently indicating to the host that the memory device is available for reading, as indicated by the read status latch and circuitry in figure 7.

18. With respect to claim 23, See *et al.* disclose monitoring the processing of the read request to determine when the circuitry has finished processing the read request, by teaching in column 7, lines 39-42, that the status may be provided automatically during read operations while the flash device remains in status mode.

19. With respect to claim 24, See *et al.* disclose commencing an operation selected by the group consisting of erasing the programming the non-volatile memory device, by the memory device, during said operation, requesting a read operation, by the host, and in response to the request, suspending said operation by the memory device, by teaching in column 3, lines 55-58, which recites a method and apparatus for suspending a non-read (erase/program) operation in a nonvolatile writeable memory in order to read code from the nonvolatile writeable memory.

20. With respect to claims 25 and 26, See *et al.* disclose that in response to said request, signaling to the host to delay execution of the request, by the memory device, in response to the signal, delaying execution of the request by the host, by teaching in figure 4A-B and in column 3, lines 15-25, enabling and disabling interrupts to allow read and non-read operations, and a check for occurrences of interrupts

21. With respect to claim 27, See *et al.* disclose signaling the host to resume execution of the request by the memory device, as indicated by the read status latch and circuitry in figure 7, and the Ready/Busy (RY/BY#) pin 62 of the flash device

22. With respect to claim 28, See *et al.* disclose subsequent to the suspending, monitoring a conclusion of the read request from the host, by the memory device, and upon detecting said conclusion, resuming said operation by the memory device, by teaching in column 8, lines 55-60, that the memory array control circuitry 140 includes a means for storing the state of the suspended non-read operation so that the non-read operation can be resumed later.

Claim Rejections - 35 USC § 103

23. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

24. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over See *et al.* and Keeley *et al.* (US Patent # 4,491,790).

25. See *et al.* teach all other limitations of the parent claim, but fail to specifically disclose code execution and data storage/processing within a bank of single memory chips with single silicon dies. Keeley *et al.* teach in column 12, lines 5-8, of an EEPROM array with two banks which is used in a system which can suspend or resume processor operations.

26. It would have been obvious to one of ordinary skill in the art, having the teachings of See *et al.* and Keeley *et al.* before him at the time the invention was made, to modify the EPROM array in the system which can suspend or resume processor operations taught by See *et al.*, to be a banked EEPROM array, as with the system which can suspend or resume processor operations

taught by Keeley *et al.*, to allow parallel access to the banks of the memory device, as taught by Keeley *et al.*.

Response to Arguments

27. Applicant's arguments with respect to claims 1-28 have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

28. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL.** See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

29. The prior art made of record on form PTO-892 and not relied upon is considered pertinent to applicant's disclosure. Applicant is required under 37 C.F.R. § 1.111(c) to consider

these references fully when responding to this action. The documents cited therein teach similar non-volatile memory devices.

30. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Matthew D. Anderson whose telephone number is (703) 306-5931.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matt Kim, can be reached on (703) 305-3821. The fax phone number for this Group is (703) 305-9731.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 305-3900.

Matthew D. Anderson
January 9, 2004

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100